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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/862,894 | 05/22/2001 | Mitsuhiro Nakamura | 09792909-5022 | 9845 |

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| EXAMINER |
|---|
| RODRIGUEZ, ISABEL |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

DATE MAILED: 07/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/862,894 | Applicant(s) NAKAMURA ET AL. | |
|---|---|---|---|
| | Examiner Isabel Rodriguez | Art Unit 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,4-6,9-10,13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuzuki et al. (US 4,760,434).

a) Regarding claims 1 and 5, Tsuzuki et al. discloses a protection circuit (Fig. 10) for a field effect transistor (22) for protection against a surge breakdown comprising a diode array (73) having a plurality of forward direction first diodes and reverse direction second diodes are cascade-connected wherein a gate electrode of the FET is grounded through the diode array.

b) Regarding claims 4 and 10, Tsuzuki et al. discloses the FET is a junction FET. See col. 3 lines 35-41.

c) Regarding claim 6, Tsuzuki et al. discloses the semiconductor device is formed on a compound semiconductor substrate. See col. 1 lines 49-51.

d) Regarding claim 9, Tsuzuki et al. discloses the diode includes a first conductivity type first impurity introduction layer and a second conductivity type second impurity introduction layer provided opposite to the first impurity introduction. See col. 6 lines 49-53.

e) Regarding claims 13-15, Tsuzuki et al. discloses a protection circuit (Fig. 10) for a field effect transistor (22) for protection against a surge breakdown comprising a diode array (73) in which a first diode has an anode connected to the gate electrode, a second diode has an anode

connected to the cathode of the first diode, a third diode has an anode connected to the cathode of the second diode, and a fourth diode has an anode connected to the cathode of the third diode. See Fig. 10.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuzuki et al. in view of Voldman et al. (US 6,433,985).

a) Regarding claims 2 and 8, Tsuzuki et al. discloses a protection circuit of a FET according to claim 1, wherein the diode is a silicon p-n junction diode. Tsuzuki et al. does not disclose that the diode is a Schottky diode including a Schottky electrode. Voldman et al. discloses an ESD protection circuit including diodes that can be chosen to be any commonly known diodes including Schottky diodes. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Schottky diodes because it would be equivalent to use the Schottky diode and thus would not affect the function of the ESD protection circuit. See col. 2 lines 36-39.

b) Regarding claim7, Tsuzuki et al. discloses a semiconductor device as described in claim 6 with a substrate composed of Silicon. See col. 3 lines 42-45. Tsuzuki does not disclose

that the substrate is made of gallium arsenate (GaAs). Voldman discloses a semiconductor composed of any semiconductor known compound such as GaAs or silicon germanium, thus establishing equivalency between both coumpounds. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use GaAs instead of a silicon compound because it has been proven to be equivalent and shall not change the function of the function of the device. The selection of known equivalents would be within the level of ordinary skill in the art.

5. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuzuki et al

Tsuzuki et al. discloses the semiconductor device according to claim 5 in which protection is provided to a junction field effect transistor. Tsuzuki et al. does not disclose that the FET is a Schottky barrier gate transistor nor a hetero junction field effect transistor. The examiner takes Official Notice of the equivalence of Schottky barrier gate transistor, a hetero junction field effect transistor and a field effect transistor for their use in the semiconductor protection art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use any kind of transistor in order to provide protection against ESD to any equivalent transistor.

***Response to Arguments***

6. Applicant's arguments filed 5/16/03 have been fully considered but they are not persuasive.

7. Regarding applicant's argument that Tsuzuki et al. is directed to a semiconductor device for protecting against overheating and that there is no disclosure of multiple pairs of diodes as

disclosed and claimed, the examiner disagrees. Tsuzuki et al. discloses protection against overheating in the circuit with reference number 100 as can also be seen in figure 3. Tsuzuki further discloses a gate-protecting unit with reference number 300. See col. 6 lines 50-55. This gate-protecting unit comprises diodes labeled 73. These diodes read on claims 1,4-6,9-10,13-15 because they provide protection against a surge breakdown. The diode array includes a plurality of forward direction first diodes and reverse direction second diodes that are cascade-connected and a gate electrode of the FET is grounded through the diode array. Two pairs of diodes are shown in figure 10 but the marks between them indicate that a further amount of diode pairs could be included.

8. Regarding applicant's argument that Voldman et al. does not disclose multiple pairs of diodes the examiner acknowledges this is true but this does not form part of the basis for rejection of the claims. With the Voldman et al. references the examiner established that the use of surge protection for various types of transistors was previously known in the art and that it is common for an ESD protection circuit to be effective in providing protection to the various types of transistor among which the FET, Schottky barrier gate transistor are disclosed and even to other types of unspecified transistors such as hetero junction field effect transistor.

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isabel Rodriguez whose telephone number is 703-305-4761. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 703-308-3119. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7704 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

IR
June 24, 2003

GREGORY J. TOATLEY, JR.
PRIMARY EXAMINER